IN THE CLAIMS:

Please amend Claims 1-8 as follows:

1. (currently amended) A pattern generator in a semiconductor test system for generating test patterns for testing a semiconductor memory device, comprising:

an inversion request signal circuit for generating an inversion request signal for each specified memory cell of a semiconductor memory device under test for inverting write data to the specified memory cell;

wherein locations of specified memory cells are on a diagonal line on an array of memory cells in the semiconductor memory device under test, and wherein ~~the~~ overall numbers of memory cells in a row (X) and column (Y) are different from each other;

wherein the pattern generator generates the test pattern that includes:

address data for accessing the semiconductor memory device under test and a failure memory provided in the semiconductor test system for storing test results therein;

control data for controlling an operation of the semiconductor memory device under test, and

write data for being written in the semiconductor memory device under test at addresses defined by the address data.

2. (currently amended) A pattern generator in a semiconductor test system as defined in Claim 1, wherein the inversion request signal circuit is comprised of:

a diagonal inversion set register for storing a set value defining locations of the diagonal lines on the array of memory cells;

an accumulator for adding Y address data for the semiconductor memory device under test and the set value from the register;

a Y AND gate provided with ~~the~~ an output of the accumulator, a maximum Y address value, and a maximum X address value;

an X AND gate provided with X address data for the semiconductor memory device under test, the maximum Y address value, and the maximum X address value; and

a comparator for comparing outputs of the Y AND gate and X AND gate and generates the inversion request signal when the outputs of the Y and ~~S~~ X AND gates match with each other.

3. (currently amended) A pattern generator in a semiconductor test system as defined in Claim 1, wherein the inversion request signal circuit operates to perform the following equation for each and every address of the semiconductor memory device under test:

(Y address of memory cell + diagonal inversion set value) AND (maximum X address value AND maximum Y

address value) = X address of memory cell AND (maximum X address value AND maximum Y address value)

wherein when the results of right side and left side of the equation match with one another, the inversion request signal circuit generates the inversion request signal, thereby inverting the write data to the specified memory cells of the semiconductor memory device under test.

4. (currently amended) A pattern generator in a semiconductor test system as defined in Claim 1, wherein the inversion request signal circuit operates to perform the following equation for each and every address of the semiconductor memory device under test:

**(X address of memory cell + diagonal inversion set value) AND (maximum X address value & maximum Y address value) = Y address of memory cell AND (maximum X address value AND maximum Y address value)*

where the mark * indicates bit inversion which inverts the data indicating the added result within the parentheses that comes immediately after the mark; and

wherein when the results of right side and left side of the equation match with one another, the inversion request signal circuit generates the inversion request signal, thereby

inverting the write data to the specified memory cells of the semiconductor memory device under test.

5. (currently amended) A pattern generator in a semiconductor test system as defined in Claim 1, ~~generates address data for accessing the memory device under test and a failure memory provided in the semiconductor test system for storing test results therein, control data for controlling an operation of the memory device under test, and write data for being written in the memory device under test at addresses defined by the address data;~~ wherein the write data inverted in response to the inversion request signal is also sent to a logic comparator provided in the semiconductor test system as expected data for comparing with output data of the memory device under test.

6. (currently amended) A pattern generator in a semiconductor test system as defined in Claim 1, ~~generates address data for accessing the memory device under test and a failure memory provided in the semiconductor test system for storing test results therein, control data for controlling operations of the memory device under test and the failure memory, and write data for being written in the memory device under test at addresses defined by the address data;~~ wherein the write data inverted in response to the inversion request signal is sent to a logic comparator provided in the semiconductor test system as expected data for comparing with output data of the memory device under test, and information

on data inversion is provided to the failure memory to be stored therein.

7. (currently amended) A method of generating a test pattern for a semiconductor test system for testing a semiconductor memory device, ~~**including a step of**~~ comprising the following steps of:

generating address data for accessing a semiconductor memory device under test and a failure memory provided in the semiconductor test system for storing test results therein;

generating control data for controlling an operation of the semiconductor memory device under test;

generating write data for being written in the semiconductor memory device under test at addresses defined by the address data; and

generating an inversion request signal by performing the following equation for each and every address of the semiconductor memory device under test:

(Y address of memory cell + diagonal inversion set value) AND (maximum X address value AND maximum Y address value) = X address of memory cell AND (maximum X address value AND maximum Y address value)

wherein when the results of right side and left side of the equation match with one another, the inversion request signal is generated to invert the write data to a memory cell

of the semiconductor memory device under test specified by the X and Y address in the equation; and

wherein locations of specified memory cells are on a diagonal line on an array of memory cells in the semiconductor memory device under test where overall numbers of memory cells in a row (X) and column (Y) are different from each other.

8. (currently amended) A method of generating a test pattern for a semiconductor test system for testing a semiconductor memory device, ~~including a step of~~ comprising the following steps of:

generating address data for accessing a semiconductor memory device under test and a failure memory provided in the semiconductor test system for storing test results therein;

generating control data for controlling an operation of the semiconductor memory device under test;

generating write data for being written in the semiconductor memory device under test at addresses defined by the address data; and

generating an inversion request signal by performing the following equation for each and every address of the memory device under test:

**(X address of memory cell + diagonal inversion set value) AND (maximum X address value & maximum Y address value) = Y address of memory cell AND (maximum X address value AND maximum Y address value)*

where the mark * indicates bit inversion which inverts the data indicating the added result within the parentheses that comes immediately after the mark; and

wherein when the results of right side and left side of the equation match with one another, the inversion request signal is generated to invert write data to a memory cell of the semiconductor memory device under test specified by the X and Y address in the equation; and

wherein locations of specified memory cells are on a diagonal line on an array of memory cells in the semiconductor memory device under test where overall numbers of memory cells in a row (X) and column (Y) are different from each other.